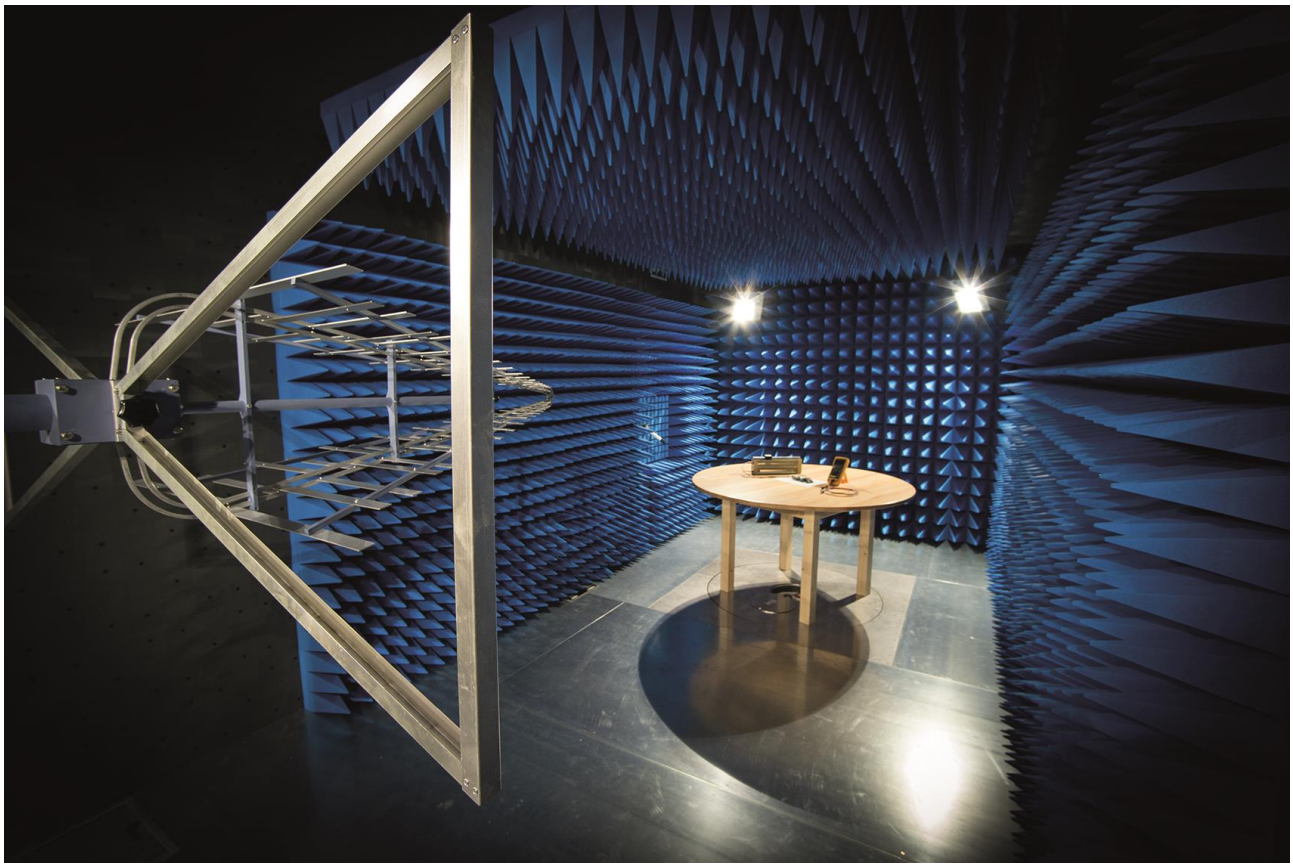
RECOM

Whitepaper

Power Supply Meets EMC



March 2016

Table of contents

List of figures

List of tables

1 Introduction

The main purpose of this document is to give a short introduction about the basic knowledge of EMC and connect this knowledge with the topic power supply. The first part is concerned with the principle as well as the definition of the topic EMC. Additionally the main test procedures which are far more than radiated and conducted emission with respect to EMC are listed and explained. So this part should provide an awareness of the vast variety of EMC-test procedures.

The second part explains a lot about coupling mechanisms, which are usually included in every EMC-Presentation. The information in this section can be applied to all EMC-issues.

When talking about power supplies and EMC, it is inevitable to mention protective devices that are necessary against transient disturbances. So the third part presents these protective devices with a special consideration when placing them.

The fourth part is concerned with the EMC-focused designs of three different DC/DC-Converters. Explaining the single measures, a connection to the second part can be made.

The last part of this paper is information gathered from experience about how to find the noise source as well as how to start with the design keeping EMC in mind. So it contains not only the information on how to handle a failed design, but also what should be done before starting the design in order to avoid slipping into the fail-situation.

2 Principles

Every electrical device emits and receives electromagnetic disturbances. So usually every device is both source and sink as depicted in Figure 1. But due to the performance of these devices, some of them are more likely to be a significant source, and some are prone to be a sink. A pacemaker, for example, is more likely to be a jamming sink than a source.

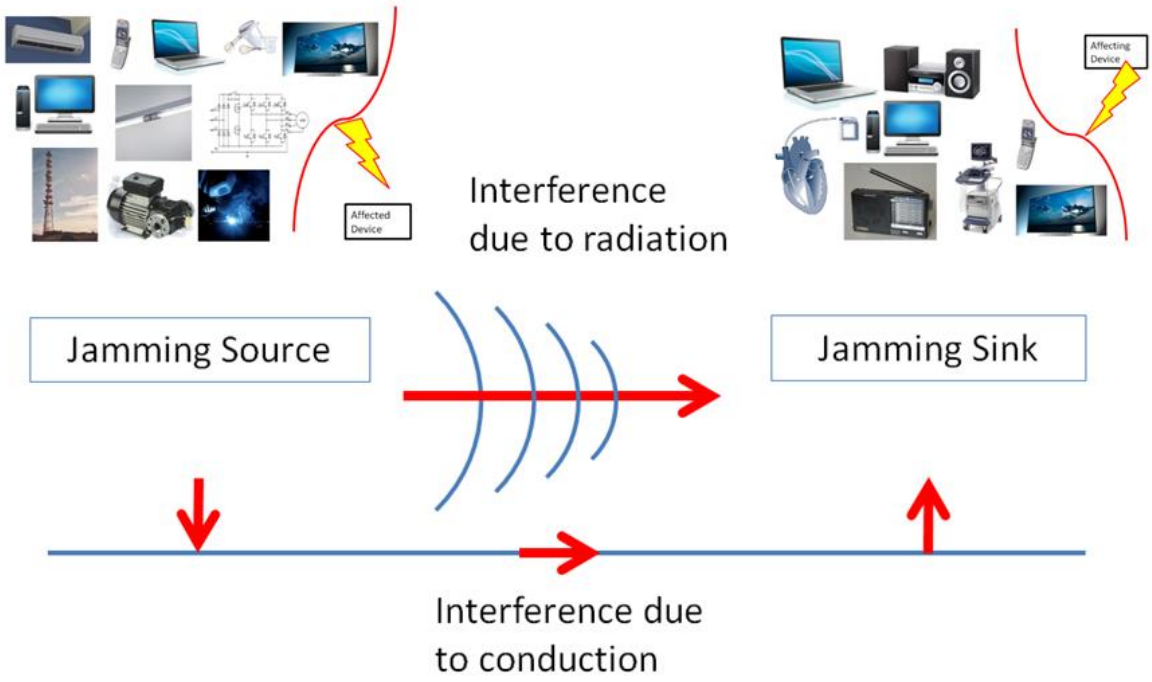


Figure 1: Principle

There are two ways to emit or receive disturbances. The first one is through free space - there is no medium necessary. Mobile phones use this phenomenon to operate. They emit encoded electromagnetic waves and also receive and decode electromagnetic waves to send and receive information. But electromagnetic waves take not only this path electric and magnetic fields can also spread and couple in into a device.

The second path a disturbance can take is over a wire, a metal sheet, or basically anything conductive. Just like with radiated emissions, several types of disturbances may occur.

Beside the frequency-dependent disturbances we measure (e.g. according to EN55022) transient disturbances such as surge, burst, and ESD exist and can cause troubles.

3 Definitions

The definition of EMC according to the EU-directive suggests that a device must be able to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to other equipment in its environment. This directive declares that devices should be not too sensitive and should reduce radiation. Additionally this directive requires that emission tests are conducted at the mode which probably emits the most disturbances, and immunity tests must be conducted at a mode where the device is most sensitive to external disturbances.

4 Typical EMC-Tests

When considering EMC-tests or EMC-issues, radiated or conducted emission often come to mind; however, there exist several additional topics to be considered. Nevertheless, experience has shown that conducted and radiated emission tests are the most critical tests the engineers must face.

4.1 Conducted emission

The measurement of the disturbing voltage in the lower frequency range between 9kHz and 30MHz in the lines going to or leaving the device is called conducted emission. The purpose of this measurement is to avoid interferences between several devices connected over cables or on the same main power line. If the tested device remains below the limit, it probably won't cause any disturbances to other equipment.

4.2 Radiated emission

The measurement of the disturbing electrical field above 30MHz is called radiated emission. The measurement is usually set up according to CISPR16. Dependent on the particular standard, the limits according to the required CISPR-standard are applied.

This measurement determines whether or not the emitted electromagnetic waves of the tested device will probably disturb any other nearby electrical equipment.

4.3 ESD

Another type of critical test covers transients for example ESD. For the ESD-test a pulse with a specific shape is applied either to conductive parts of the device itself, conductive metal parts nearby with a specific distance and setup, or to nonconductive but touchable parts of the device. These pulses usually cause E-Fields in the systems that might lead to an interrupt, a shutdown, a reset, or any other unwanted behaviour. Therefore, the device should be designed to be robust against these electromagnetic phenomena. Depending on the typical environment in which the device is used, different test levels are valid if not mentioned otherwise in a particular standard.

The ESD-pulse is quite high (up to +/-15kV) and very fast (ns-range). Due to the very fast pulse applied directly and indirectly to the device, this test is one of the most critical of all EMC-tests.

4.4 Surge

The surge test applies a pulse with a specific shape over galvanic coupling onto the lines of the tested device. The purpose is to test the robustness of the device against indirect lightning strikes. Unless otherwise stated, the test levels must be applied according to the environment in which the device is used.
The pulse of the surge test is not very high (up to +/-4kV) and very slow (µs-range), which leads to a high amount of dissipated energy. This high energy is the critical part of this test which easily leads to a damaged device.

4.5 Burst

The Burst test has a property of the surge and ESD tests. The pulse itself is very fast (ns-range) like the ESD-pulse, but is much lower (about maximum +/- 4kV) like the surge-pulse. However, this pulse is repeated over a fixed period of time at a specific interval.
The Burst-test simulates the brush-sparking of a motor. Even though the pulse is fast with a rise time in ns, since the coupling is capacitive, the device does not have to directly drain the current, this is the least harmful of the transient tests.

4.6 Harmonics

The harmonics test is one of the most important tests that we have to cope with as a power supply distributor. This measurement indicates if there is a harmonic distortion superimposed onto the fundamental frequency of 50Hz.

4.7 Flicker

A device consuming very high energy for short periods of time can cause voltage dips which may cause problems with other devices connected to the same mains powerline. If this happens too often or the influence is too high, the device won't pass the flicker test. Therefore this test may be critical for devices switching high energy in short intervals. The value for the pass or fail criteria once was determined empirically and is dependent on the magnitude of the drop and the frequency the event occurs. The voltage drop caused by the device is allowed to occur many times per second if the drop is small, and if the magnitude of the drop is large, then it is only allowed to happen at very low frequency.

4.8 E-Field immunity

The E-Field immunity test is complementary to the radiated emission test. Here the device is tested if it is immune to external electrical fields that can be produced by other electrical equipment. The test is typically performed in a frequency-range from 80MHz to 2700MHz. The applied field is an amplitude modulated signal with 80% modulation at 1kHz.

4.9 HF-induced disturbances

Here, high frequency disturbances are induced to the lines connected to the device. The purpose of this test is to analyse the robustness of the device against external disturbances caused by other equipment connected to the same electrical system as the device. HF-induced disturbance test is often considered an important compliment to the conducted emissions test.

4.10 Voltage dips, variations and interruptions

This test determines how an electrical device behaves when the main power supply voltage changes. There are three different parts of this test, each with different types of voltage variations.

The response criteria which specify how the device should behave in response to voltage fluctuations must be selected. For example, depending on the application of the device, it may be allowed that the device shuts off in response to a voltage fluctuation. Or it could be required that the device remains operational in spite of voltage fluctuations.

Voltage dips are applied to check the influence of an abrupt voltage drop on the device.

4.11 Magnetic power field

The power magnetic field test simulates a homogenous magnetic field with the frequency of the main power supply – 50Hz/60Hz. The device, when placed in a magnetic field typically produced by a Helmholtz coil, has to work properly. Devices like cathode tube monitors were very affected by this test.

5 Types of coupling

The following figure shows a model where Rk, Ck, and Zk represent parasitic elements responsible for coupling in a circuit. Galvanic coupling is depicted by the resistor Rk. Parasitic capacitive coupling is represented by the parasitic capacitance Ck. Parasitic inductive coupling is represented by the parasitic elements Zk.

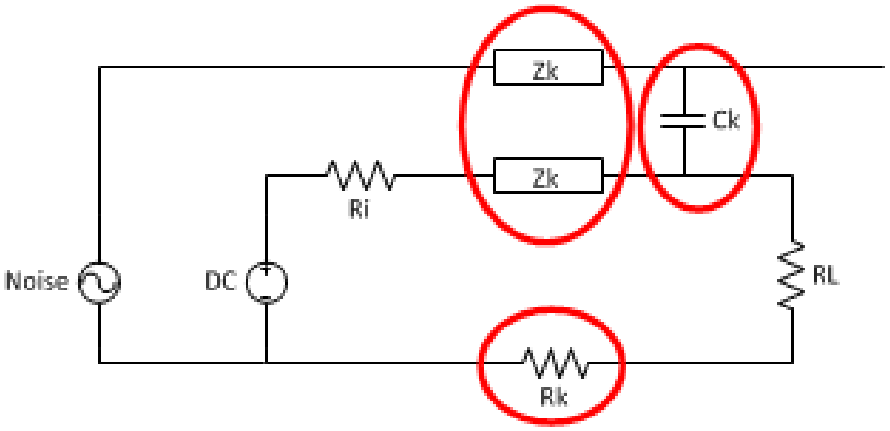


Figure 2: Coupling Mechanism

The only coupling mechanism not pictured in Figure 2 is the airborne coupling since it can't be sketched via parasitic elements.

5.1 Galvanic coupling

Figure 3 shows a circuit branch with a supplementary noise signal represented by a resistive value. The noisy current in the circuit creates a noisy voltage on the parasitic resistive trace, which affects the voltage on the resistive load. In this case, an ideal source can become a noisy source due to the addition of noise on a common branch.

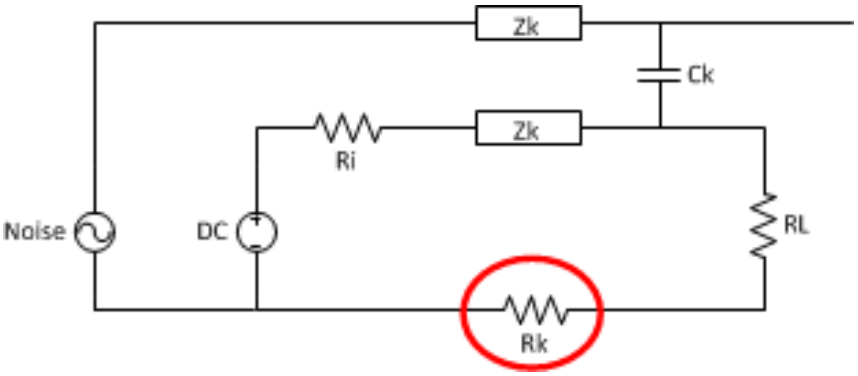


Figure 3: Galvanic Coupling

Measures

This type of coupling can be reduced by decreasing the impedance and therefore the common resistive path of the two circuits since the effect on the voltage on the resistive load is directly proportional to the impedance of the common trace.

If the location and source of the noise is known, the noise current itself can be reduced. This can be accomplished by reducing the noise directly at the source, by using a filter so that the noise is reduced on its path to the jamming sink, or by reducing the frequency of the noise. The effect of the impedance of the common trace is directly proportional to the frequency of the noise since impedance is a frequency-dependent value. The frequency in a system should be as fast as necessary and as slow as possible.

To avoid a common trace, a star-point topology can be used for several circuits in order to separate the noisy part from the load-circuit. The ground systems are connected at one single point.

To avoid uncontrollable coupling the return path should be considered as well as the forward path when doing the layout. As the design usually consists of several forward and return paths, every single path should be prioritized and categorized as aggressive, sensitive, or indifferent traces.

The most aggressive loop has the highest di/dt, which means it should be as small as possible and have the highest priority among the aggressive traces.

5.2 Capacitive coupling

The parasitic element Ck in Figure 4 is present in circuitry between adjacent wires in parallel. Over this capacitance, which is usually very low, HF-signals may couple to other components and become problematic.

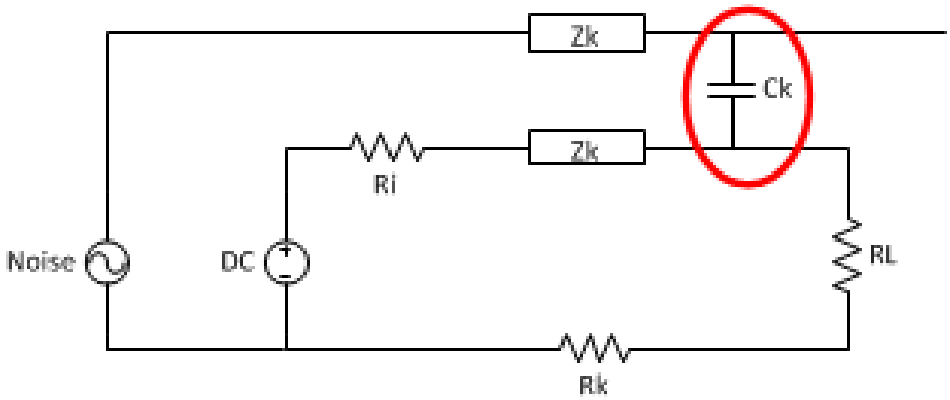


Figure 4: Capacitive Coupling

Measures

Several measures may be made in order to reduce capacitive coupling:

- Short traces are one countermeasure to deal with capacitive coupling since the length of the trace is directly proportional to coupling of the conductive parts. Traces in parallel over long distances are more prone to capacitive coupling which may become problematic for (for example) an analogue measurement line in parallel to a clock line.
- Additional capacitors create symmetry for very sensitive signals so that the noise is coupled back early on before the noise can cause trouble.
- Capacitive coupling can be reduced by shielding with conductive material.
- The capacitive coupling can also be decreased by reducing the frequency.
- In the case where cables are ran over large distances, twisted pairs (possibly shielded) are very helpful in order to avoid unwanted coupling.

5.3 Inductive coupling

Live wires can be inductively coupled via magnetic fields. These fields can couple into nearby metal parts (which might be sensitive traces) and induce current.

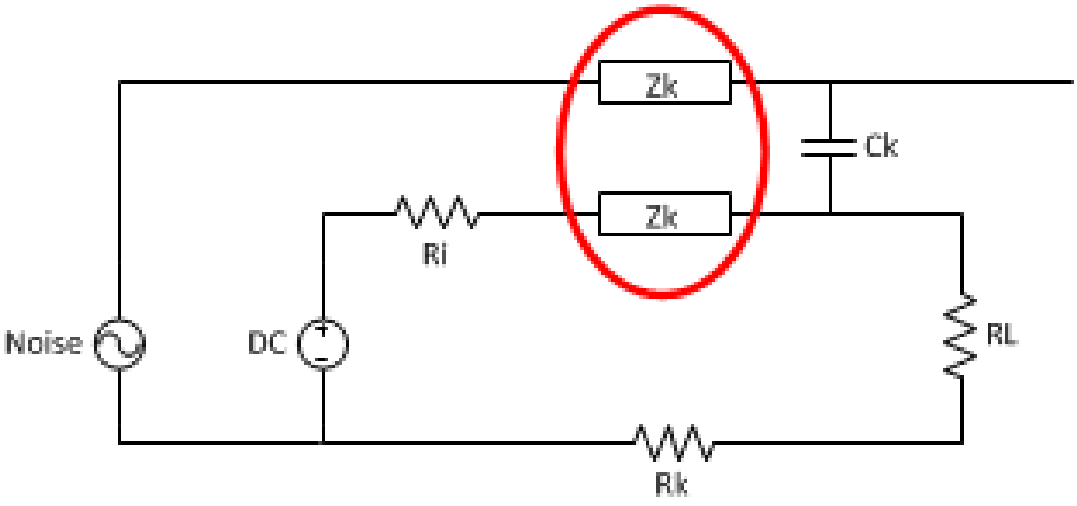


Figure 5: Inductive Coupling

Measures

Several measures may be made in order to reduce inductive coupling:

- Like with capacitive coupling, traces for different signals should not be designed in parallel since live wires in parallel induce current in one another.
- Large loops in noisy circuitry produce large magnetic fields, so the most critical loops with the highest di/dt should be designed as small as possible. Additionally, very sensitive loops should be small as well since circuits with larger loops are more prone to disturbances.
- In order to design small loops, the designer must always consider the return path.
- The traces are less sensitive to frequencies when the loops (and therefore the impedances) are small.
- As the frequency is reduced, so is the inductive coupling. A design should have a frequency which is as slow as possible and as fast as necessary.
- There is also a way to shield magnetic fields with nonconductive materials such as perm alloy and µ-metal which may be found in RFID and NFC- applications.
- Ferrite plates may be used on controllers to shield magnetic fields.

5.4 Airborne coupling

Radiated emission measurement is a form of airborne coupling. If the measured emission is very high, then there is a high level of coupling between the EUT and the antenna. Since the antenna should not be altered, the coupling can only be modified by shielding the device. There are two different measurement types for radiated emission. Typically radiated emissions are measured in µV/m, and normal metal shielding is sufficient; however, when measuring according to CISPR11 Group 2 devices, the H-field is measured in µA/m.

Depending on the size of the device under test and the length of the cables, the emission usually appears at $\lambda/4$ of the wavelength. In most cases, the cables work as antenna while the source is on the board.

Either shielded cables or filtering before the cabling can reduce the radiated emission. Regardless, every outgoing and incoming signal should be filtered.

Radiated emission also decreases at lower frequencies, which in turn lowers the airborne coupling of the device and the antenna.

6 Protective Elements

Protective circuitry is one of the most important subsystems for AC/DC converters. These elements must protect the device against surge, burst and ESD.

There are several possibilities to protect the device:

- Spark air gaps, which can dissipate most of the additional energy
- Gas discharge tubes
- Varistors

For protecting ICs with much smaller amplitudes, a suppressor-diode or Zener-diode is the right solution.

All of these elements are important to consider since each device has its voltage and energy range where some or all of these elements should be used. For power supplies, normally two or even three elements are used since the energy pulses can be very high.

An element that can convert higher energy also allows a higher amount of energy to pass; for example, the spark air gap can remove the highest energy, but will not be able to reduce the voltage to a safe level. The gas discharge tube can remove less energy but will reduce the voltage lower than the spark air gap. The same holds for varistors, diodes, etc.

This leads to the optimal placement shown in Figure 6. The current firstly passes the device with the ability to take the highest energy. The residual voltage, which is still quite high for the circuitry, will be taken by the next device, which might be a gas discharge tube or a varistor. This device reduces the residual voltage to a lower value.

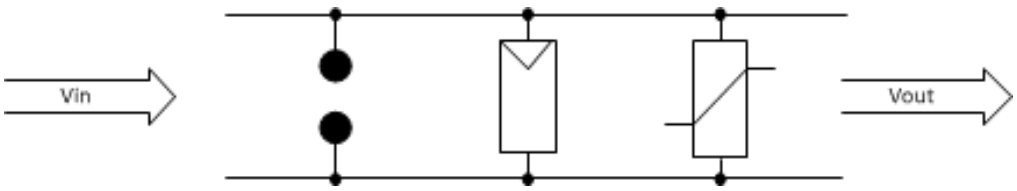


Figure 6: Protective Elements

If the components are placed the other way round, it might be possible that the first device dies because it cannot sustain such a high energy, and the second element does not work because the first device already created a short-circuit.

7 AC/DC Power Supplies

What do AC/DC power supplies have to do with EMC, and why do we need AC/DC converters? The main power-supply line usually supplies every electrical device with alternating voltage with a value between 90V and 240V typically at 50Hz or 60Hz; however, many devices such as (for illustrate)personal computers, need DC-voltages like 3.3V, +/- 5V, 12V and GND (which is usually 0V). This situation is sketched in Figure 7.

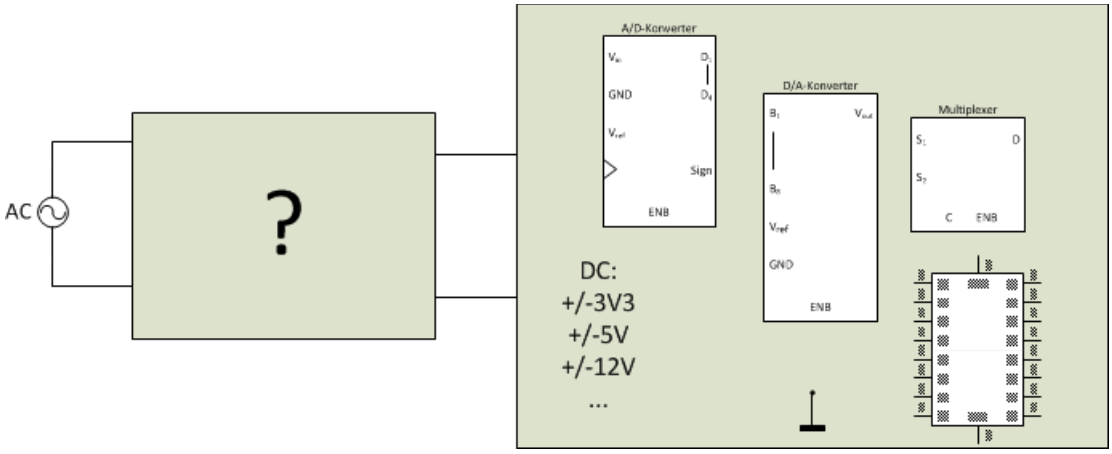


Figure 7: AC to DC

7.1 Old Solution

To generate a voltage lower than the input voltage, a typically large transformer like the one in Figure 8, was used. Nevertheless the transformer was also a large filter to eliminate disturbances transmitted between the inside of the device and the main power supply line.

The transformer had a fixed ratio to reduce the voltage and couldn't be used for wide-ranged inputs; therefore, several different options were required for different regions of the world.

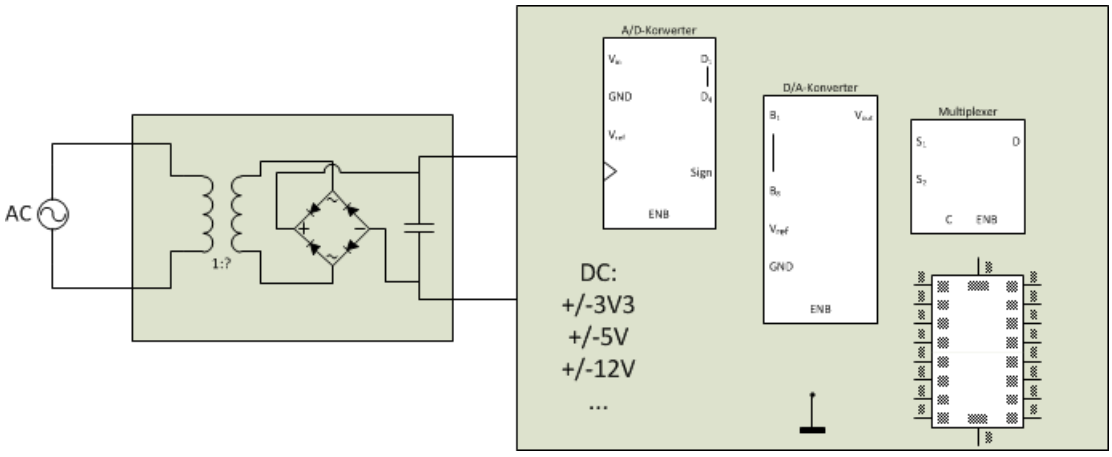


Figure 8: Old Solution for AC/DC

7.2 New Solution

Since recent improvements in semiconductor technology, switching devices have become better in switching high voltages and currents, allowing the transformer to be completely omitted from the design (Figure 9).

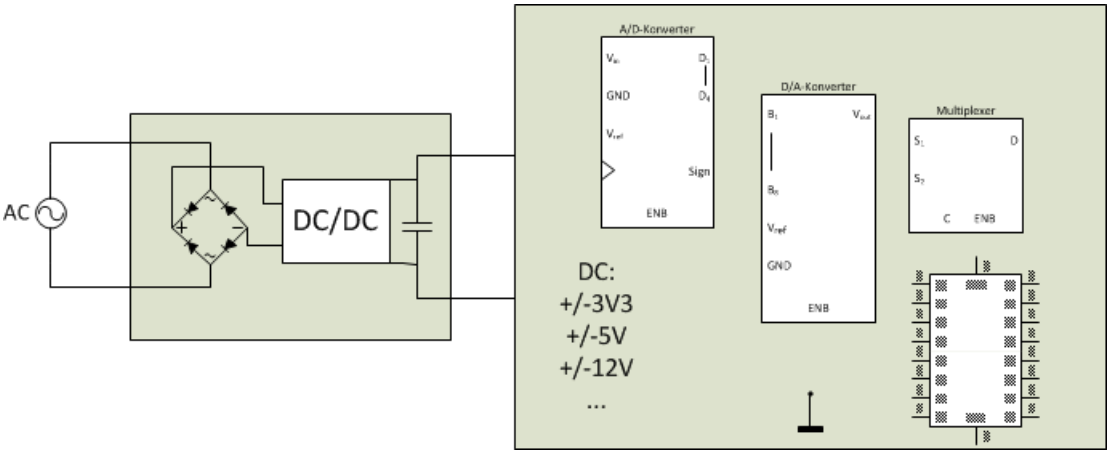


Figure 9: New Solution for AC/DC

Since the advantages listed in Table 1 outweigh the disadvantages, switching power-supplies are now more common in industry.

Advantages	Disadvantages
Arbitrary Voltage	EMC Issues
Lightweight	Poor Heat Dissipation
Effective	
Wide Input Range	
Low-cost Production	

Table 1: Advantages and Disadvantages of Switching Power Supplies

The next sections will go into detail on how to deal with EMC issues caused by switching power supplies in order to pass EMC tests.

8 Switching Power Supply Topologies

This first design suggestion to improve EMC performance is valid for every topology. In the following analysis the critical loop is identified (Figure 11). Placing conducting traces or planes below this critical loop can cause inductive coupling which transmits the noise throughout the circuit.

8.1 Boost Converter

The boost converter (Figure 10) is a DC/DC-converter without galvanic insulation.

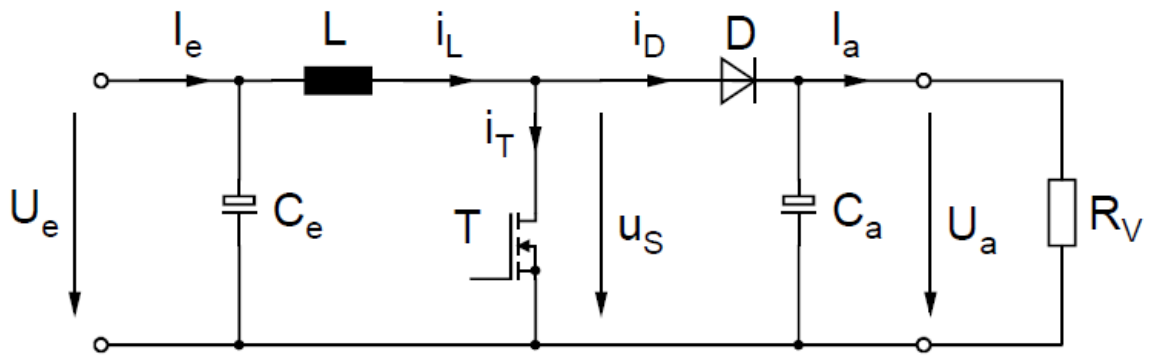


Figure 10: Boost Converter (Schematic) [2]

The output voltage is higher than the input voltage. When analysing this topology in regards to EMC, it's necessary to identify the switching node and the critical loop.

In Figure 10, du/dt has the highest value at the switching node, where the components L, T, and D join. The critical loop is the loop with the components T, D, and Ca. Because it has the highest di/dt, it should be as small as possible in order to minimize the inductance and therefore the coupling to other components. Additionally the Ce should be placed close to the switching circuitry.

Analysis

The critical loop of a boost converter is shown in Figure 11.

The path from b to c is part of both the critical loop and the outer loop. Due to this common path, the high switching frequency will be galvanically coupled to other sub circuits connected to the outer loop.

To reduce the differential mode noise in Figure 11, an inductor (LF,A) was added at the output.

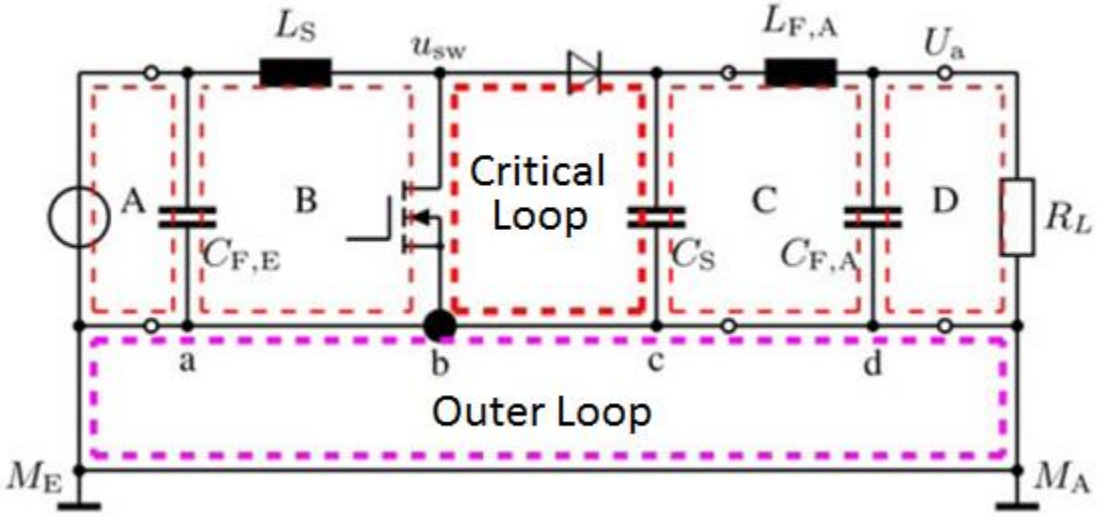


Figure 11: Analysis of the Schematic of a Boost Converter [1]

The functional schematic from Figure 11 is optimized in Figure 12. The star point BP in Figure 12 helps to avoid the coupling between the single loops in this circuitry. As a result of adding the star point, the common path of different circuitries was reduced to zero. The critical loop has to be as small as possible to reduce the impedance and magnetic field.

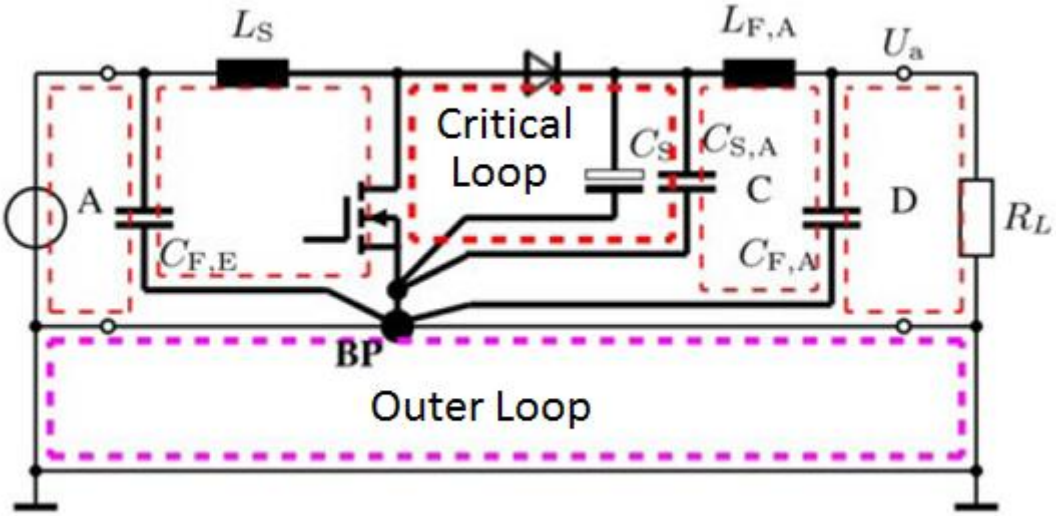


Figure 12: EMC-optimised Schematic [1]

The capacitor CS in Figure 11 is split into two capacitors CS and CS,A in Figure 12. This output capacitor stores energy and smooths the voltage ripple. Electrolytic capacitors are the best solution, but they are poor at coping with high frequency signals produced by the switching node. This is why an additional capacitor approximately 100nF with very good dielectric properties (NP0) should be used. This capacitor does not

store much energy, but it couples back the HF-current which would otherwise spread across the entire board.

The CF,A and LF,A (Figure 11 and Figure 12) are for filtering purpose to reduce the differential mode noise produced during switching.

At the transition of the switch from blocking to opening, the diode is conducting as long as the junction is not cleared out. So the capacitor is short circuit over the open diode and the open FET, causing the current in the critical loop to rise. To minimize this current, there are several solutions:

- The diode needs a very short recovery time (fast recovery, Schottky diode)
- Low slew rate at switching on (disadvantage is high dissipations and lowered efficiency)
- Additional inductor to slow this effect down

8.2 Buck Converter

The Buck-Converter (Figure 13) is a non-galvanic insulation, which generates an output voltage lower or equals the input voltage.

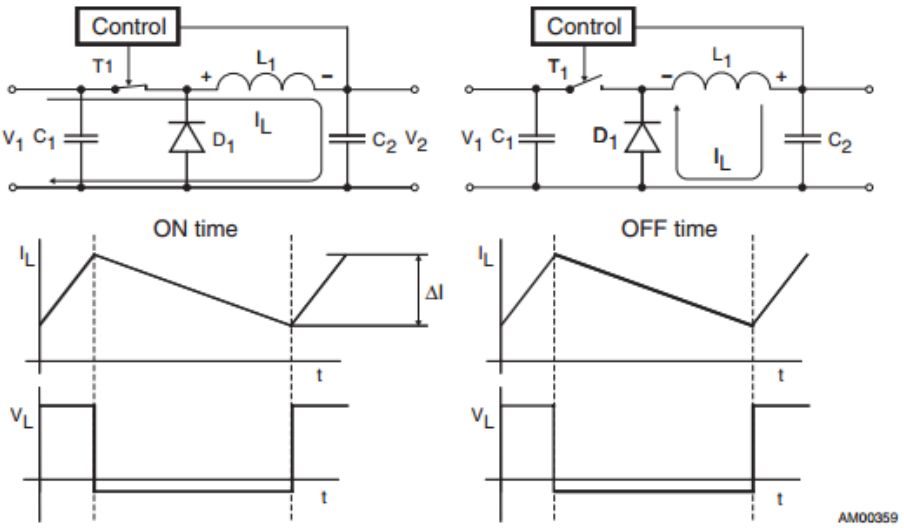


Figure 13: Buck Converter (Schematic) [3]

This topology is not recommended for Power Factor Correction (PFC), as it is high side switched what means a voltage greater than the input voltage is needed. Furthermore it is not recommended as PFC for EMC-reasons, as the switching node is connected directly to the input via the switch and there is no coil in between as e.g. in the topology of the boost converter.

Analysis

The critical loop (D,L, and C) in Figure 13 is the part with live wires in both switching stages. Again, this loop has to be done first designing the layout, before anything else, because it has to be the smallest loop possible. To avoid coupling the loops close to the critical loop have to be very small too.

Introducing a star-point as in the example before with the boost-converter is also necessary to eliminate galvanic coupling as far as possible.

Already mentioned in the section about the boost-converter the output capacitor should be split in two types – one electrolytic capacitor for storing the energy and the second one with very good dielectric properties for short circuiting the HF-noise.

Buck-Converter with Resonant Circuit

In special cases a resonant circuit can be used to reduce the noise emission of a buck-converter. In Figure 14 the schematic of this type of buck-converter is shown with the voltage and current diagram in Figure 15.

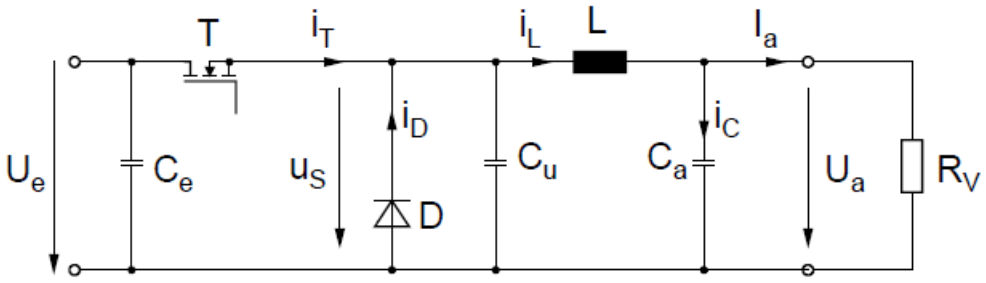


Figure 14: Buck Converter with Resonant Circuit (Schematic) [2]

The voltage and current diagram in Figure 15 shows there are no abrupt rise or fall times, but they are smooth. So this is the reason for the improved EMC-behaviour.

Anyway, to use this type of buck-converter several restrictions has to be met. One of these restrictions means that the output voltage has not to be lower than half of the input voltage. If the output voltage drops below half of the input voltage, the system becomes unstable. Using this kind of circuitry the converter has to work in critical conduction mode that means the switching frequency is load dependent. Therefore the filter, which might be needed anyway, has to be designed for broadband applications.

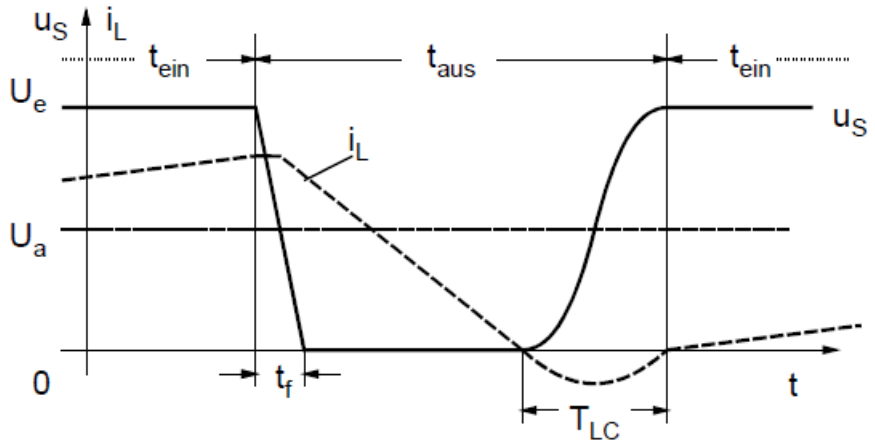


Figure 15: Voltage and Current of Buck Converter with Resonant Circuit [2]

8.3 Flyback Converter

The Flyback Converter is a galvanic insulated converter. The Inductor in this topology has a primary and a secondary side as shown in Figure 16.

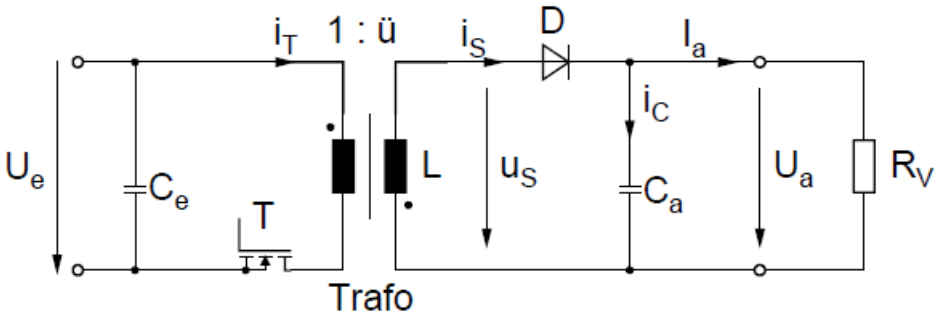


Figure 16: Flyback Converter (Schematic) [2]

To improve the behaviour regarding EMC, the critical loop has to be found. As this topology has a primary and a secondary side, two critical loops exist as outlined with thick red dashed lines in Figure 17. The mash signed with A in Figure 17 is the critical loop if the primary side, that has to be as small as possible, like already mentioned in the section about other topologies. The critical loop at the secondary side is signed with B in Figure 17. This loop as well has to have the highest priority in the design, to be as small as possible. Designing the layout the way that both loops are very small the parasitic current flow in loop signed with C is smaller and so the coupling is reduced.

Additionally the output capacitor Cs should be split again in two physical capacitors, one electrolyte capacitor to store the energy and one ceramic capacitor with good dielectric properties to short circuit the HF-noise.

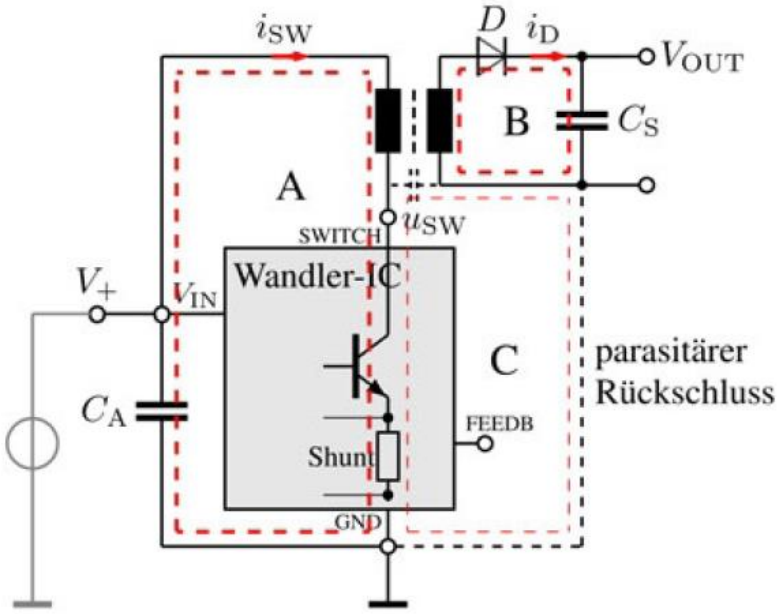


Figure 17: Critical loops of Flyback Topology [1]

8.4 Control Circuitry

This measure is applicable to every device and can be really supportive in designing a DCDC converter. Every converter usually uses a FET for switching.

The ringing visible in Figure 18 usually causes EMC-troubles; it's the ringing you see between drain and source that couples over the transformer to the secondary side. The main problem is not the signal itself, but the ringing at the beginning and at the end of the high signal.

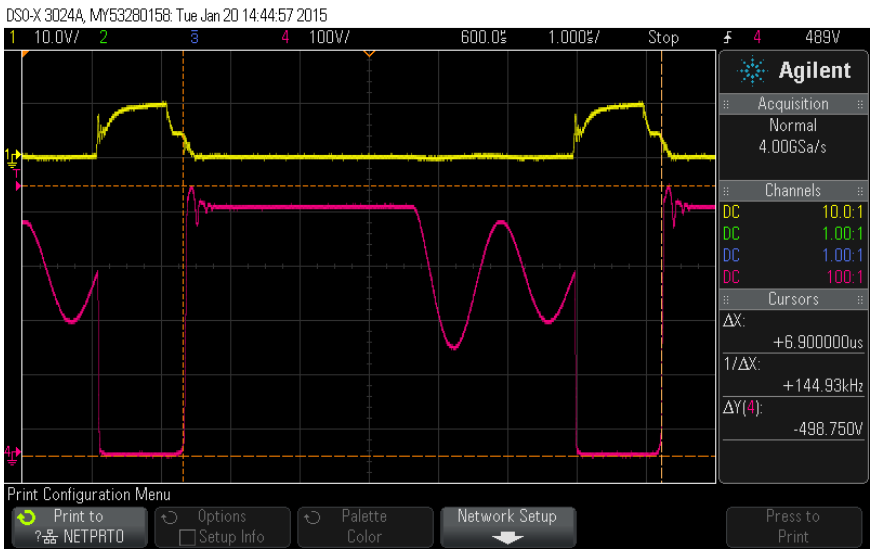


Figure 18: Ringing

The height and durance of this ringing is dependent on the rise and fall time. The shorter this time is the worse the ringing usually is. To increase the rise and fall time the resistors in the gate-control-circuitry shown in Figure 19 can be increased.

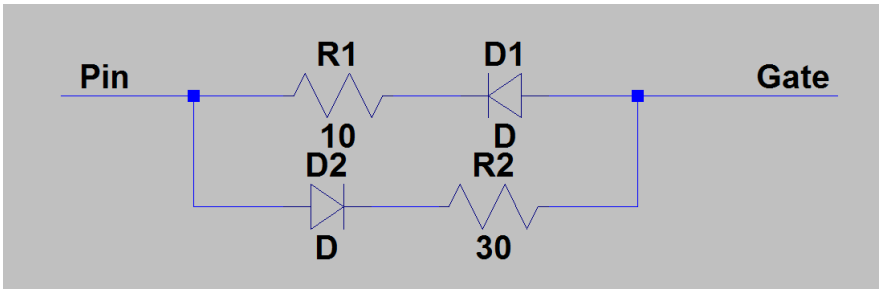


Figure 19: Additional Gate-Control-Circuitry

The path over D1 and R1 in Figure 19 is responsible for the ringing at the rising edge and the one over D2 and R2 can change the ringing on the falling edge.

Nevertheless, this method should be handled carefully, as the power dissipation increases. This might destroy the FET, if not chosen properly. It's a nice and effective tool to cope with the EMC- issue in DC-DC designs.

9 PFC

PFC is the abbreviation for Power Factor Correction that should reduce the reactive power consumption of electrical devices. Up to 75W usually the power factor does not matter according the standard IEC61000-3-2 for harmonics.

The measurement of harmonics determines the emission of multiples of the basic frequency of the main power system up to the 40th harmonic.

The PFC is an additional DC/DC-Converter places between the rectifier and the main DC/DC-Stage as shown in Figure 20.

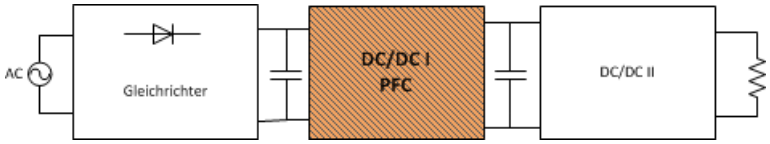


Figure 20: AC/DC Converter with PFC (Block diagram)

The main purpose of the PFC is to convert the pulsed current flow shown in Figure 21 through the rectifier into a sine shaped waveform shown in Figure 22.

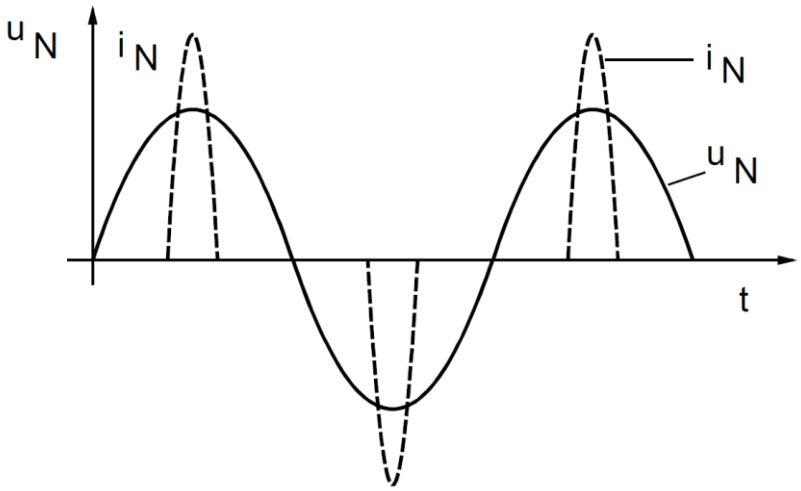


Figure 21: Without PFC [2]

A current flow like sketched in Figure 21 causes lots of harmonic emissions. The result is high reactive power consumption. For devices consuming less than 75 W this is allowed, but for devices consuming more than 75 W, the power factor correction has to be implemented to achieve a sine shaped current flow shown in Figure 22.

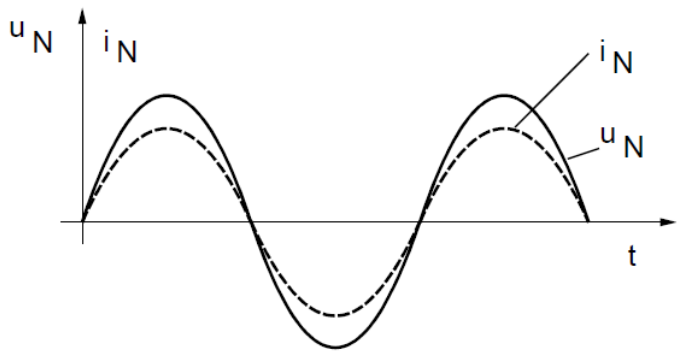


Figure 22: With PFC [2]

Modes

There are three different modes are available for PFC and therefore also for every single DC/DC-Converter. Nevertheless not each mode is recommended for every DC/DC-Converter in every application.

The continuous conduction mode shown in Figure 23 is usually used for devices consuming more than 250W. Devices with a lower power rating use either the critical conduction mode shown in Figure 24 or the discontinuous conduction mode shown in Figure 25.

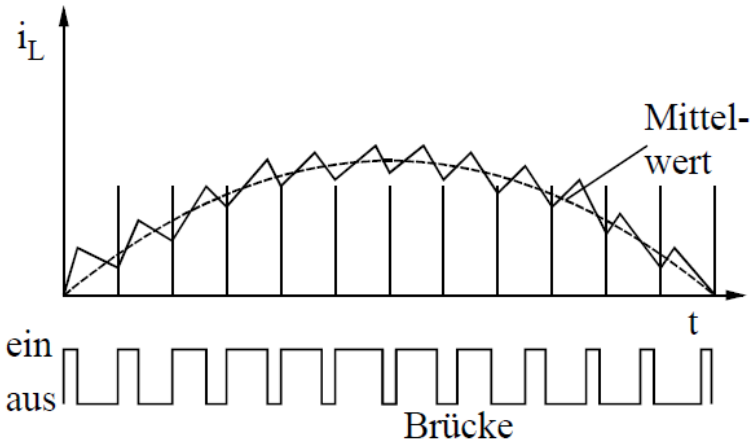


Figure 23: Continuous Conduction Mode (CCM) [2]

The main advantage of the DCM over the CCM and CRM is, that the used filter can be a very narrowband band filter, as this mode only uses on frequency. Changes of the load will be handles with a change in the duty cycle.

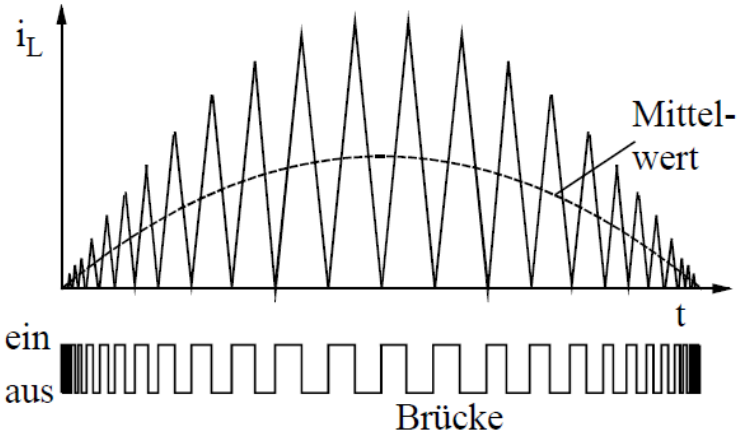


Figure 24: Critical Conduction Mode (CRM) [2]

A decision maker between DCM and CCM could be the fact, that the controlling algorithm for the discontinuous mode usually is quite easy for boost converters. Boost converters driven in critical conduction mode are quite instable and critical to implement.

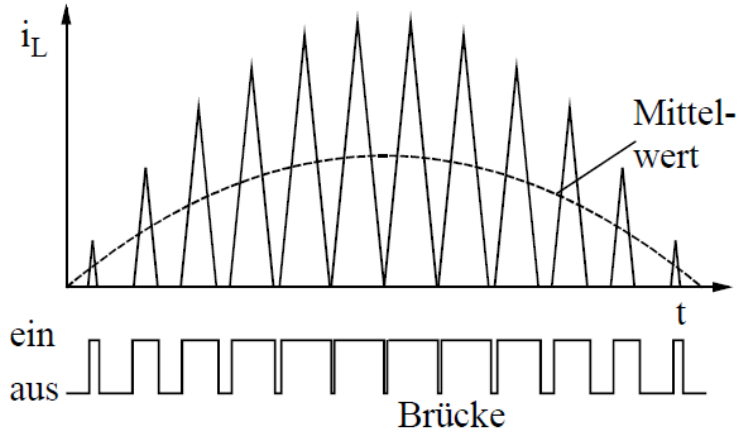


Figure 25: Discontinuous Conduction Mode (DCM) [2]

Anyway in each mode a filter will be necessary to pass the conducted emission and harmonics test. Usually the main issue is the differential noise caused by the switching regulator. Therefore a series inductance will be inevitable.

10 Action List

As the prototype is finished the EMC test will be performed. What should be done, if it does not comply with the EMC-standard? The main problem is that it is usually unknown what is responsible for the failure.

This section describes how to find the source and how to handle the emission.

In the first step the disturbing circuitry can be found by activating and measuring each circuit part separately. If this is not possible the spectrum has to be observed very carefully when turning on the device. The moment the emission exceeds the limit might be at the moment a specific component of the device becomes activated. Probably the emission exceeds the limit when display shows the blue coloured background. This very important information is necessary to figure out, which component causes troubles.

If the source is found, it should be possible to focus on that area separately. After this part becomes quiet it can be connected to the rest of the device. If this part was the only one making noise the emission should not exceed the limit any more. If it does anyway, there might be an additional noise source, which should be made quiet.

If the source is found, the type of disturbance has to be determined. Using different types of filter can identify different sort of disturbances. Using a clip ferrite on a cable gives information that the disturbance is a common mode noise if the effect is very high. Otherwise the disturbance is probably a differential noise.

Another possibility to figure out the noise source is to scan the device with nearfield probes. The area, where the highest noise level with similar spectrum waveform to far field is visible, is very probably the noise source. Next a needle probe is used to scan until the precise component or trace, which is the root cause, is found.

Having the source found means the start of real work on eliminating the noise. In some cases it is possible to eliminate the noise by changing the software for example by activating the spread spectrum mode. In general the first attempt should always eliminate the noise at the source side.

However, this is not possible very often, so the second best solution is to reduce the noise on its path or change the return loop. This can be achieved with filter components or shielded cables.

Targeting a redesign, the grounding concept should be reconsidered. Using additional planes for ground and power supply can reduce the electromagnetic emission especially in the higher frequency range about some tens MHz as visible in Figure 26. This figure shows the dependence between frequency and the probability of a specific kind of disturbance as well as the most probable solution for this disturbance.

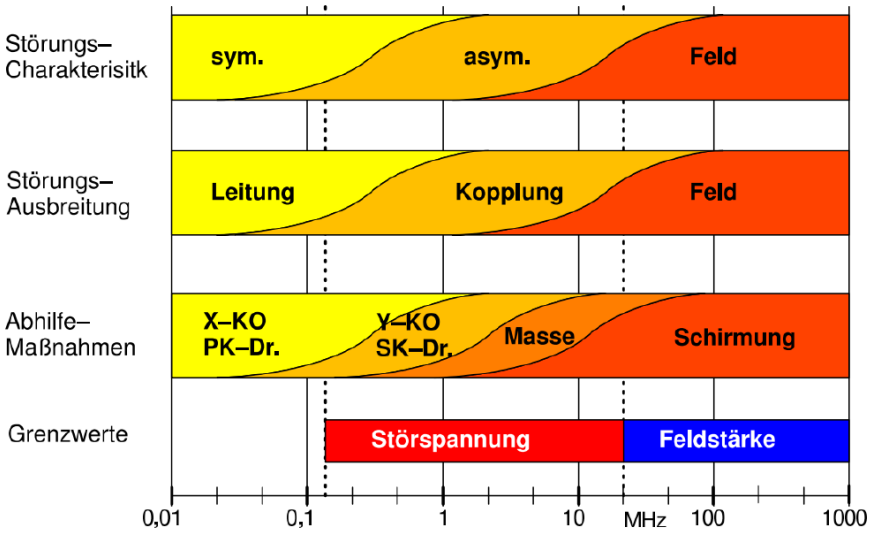


Figure 26: Frequency-dependent Solutions [4]

For a quick test the ground plane or shielding can be added by using a copper foil.

Having troubles with disturbances emitted by cables can be reduced by using shielded and/or filtered wires. Even DC-Supply cables can cause radiated and conducted emission when carrying HF-noise additionally.

After all these quick fixes the emission should be reduced below the limit. If not, a redesign might be inevitable. In this case all design-Rules listed in the next section can be checked and implemented if necessary.

An additional note mentioned here: If the EUT behaves unpredictable, triggers random resets or goes into an unidentified state, it is very likely there is an internal EMC-issue on the boards. Probably some signals couple into very sensitive signal or reset lines.

11 Analysis

11.1 Concept of areas

When starting a design the first step should create a concept of areas which separates critical from non-critical areas.

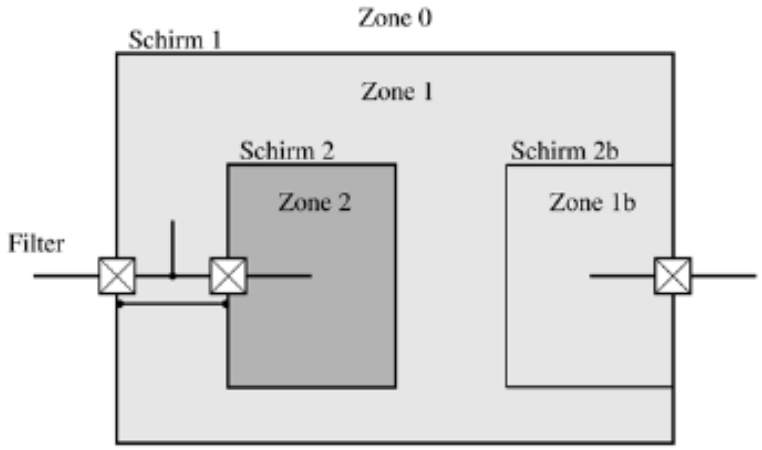


Figure 27: Concept of Zones [1]

If signal-lines from one zone enter another zone, these lines have to be filtered. The area of each zone has to be shielded against other zones. With this concept every disturbance in one zone does not affect another zone.

Additionally the signal-lines have to be sorted in three categories: disturbing, sensitive and indifferent. To trace different signal types in parallel should be avoided. Otherwise there is a non-negligible risk of coupling different signals into other traces. Different types of signals should be routed orthogonally as far as possible.

11.2 Connectors

When starting with the design, the placement of the connectors still can be considered in the block-diagram. The best solution would be like the mainboard industry already does, placing all connectors on one side of the board.

Placing the output connectors on the opposite side of the input connectors, the system can be considered as dipole antenna that leads to a much higher radiation.

Designing a shielded device it would be recommended to use shielded connectors and shielded cables. So ever signal leaving the device is shielded and the emission level will be reduced. To take the whole advantage of shielded connectors it is essential to provide a conductive contact over the whole area of the connector and to avoid any slot.

Additionally every trace leaving or entering the board has to be filtered via a capacitor against GND.

This filtering is inevitable, especially when shielding is impossible. In that case a more sophisticated filtering might be necessary.

In case that no shielding and no filter on the board are possible, the EMC-measurements will result in a failure and the only solution might be very expensive clap-ferrites.

In Figure 28 the connections shown on the left side have to be avoided and exchanged against solutions shown on the right side.

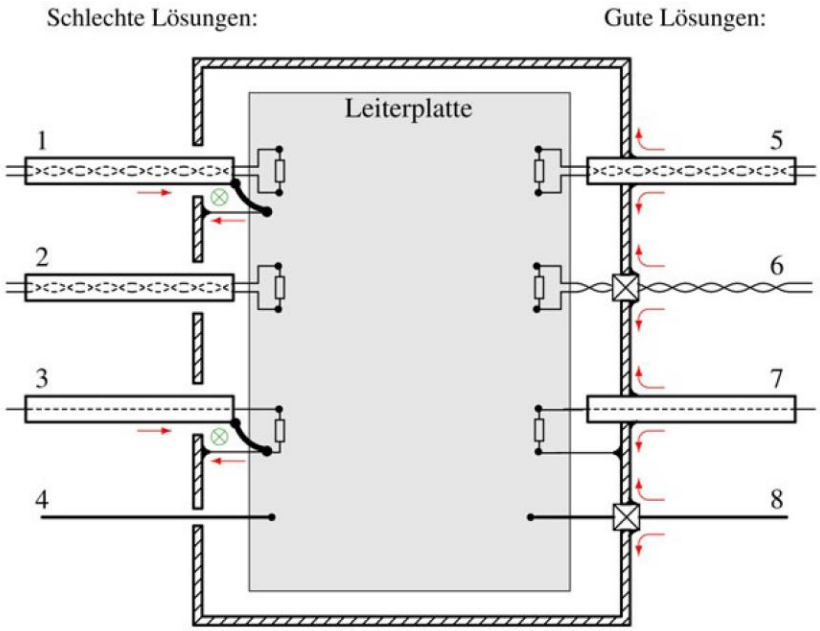


Figure 28: Bad Connections vs. Good Connections [1]

11.3 Sensitive Traces

Sensitive Traces lead over a greater distance can be protected against noise with a serial resistor. If this recommendation is ignored, the behaviour of the EUT can result in some unspecified mode, due to a reset trace susceptible to the noise nearby.

Differential traces have to be considered separately. For this type of traces special rules are applicable. One of the most important aspects is the impedance and the length of these traces, which should be Symmetrical. Meanwhile, to avoid crosstalk between the differential traces and other trace that is close to differential traces we could route a ground trace along the whole area of differential trace, through this way we can get benefits in ESD and radiated measurement.

11.4 Capacitors on stubs

Capacitors between two lines are usually used to short-circuit the HF-signals. This will be the effect when placing the capacitor correctly. Placing Capacitors on stubs will avoid this effect. Figure 29 shows an example for placing a capacitor on a stub. Here it is visible that the HF-signal would have to take an extra path to reach the capacitor. In that case it would reach the pin of the chip before the capacitor. This might lead to disturbances on the chip. The capacitor might have a positive influence anyway, but it cannot take its full effect.

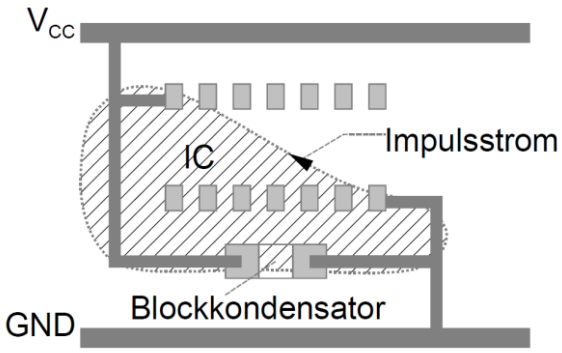


Figure 29: Cap on Stubs [2]

To improve that behaviour the literature suggests a layout shown in Figure 30. This change in the layout will improve the effect of the capacitor, but is not the best solution. The improvement will be due to the lower impedance to the capacitor that means a shorter path for the HF-signal to the capacitor. Nevertheless the HF-signal will pass the pin of the chip before being short circuit at the capacitor. Therefore a way has to be found to force the HF-signal over the capacitor before reaching the pin of the chip.

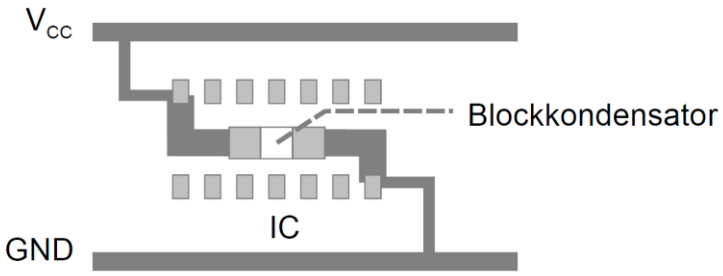


Figure 30: Shorter Traces to the Capacitor [2]

Figure 31 shows an improved layout based on the solution visible in Figure 30. This layout forces the HF-signal over the capacitor before reaching the pin of the chip. If the capacitor is effective in the frequency range of the HF-signal, this will be a short circuit before reaching the chip.

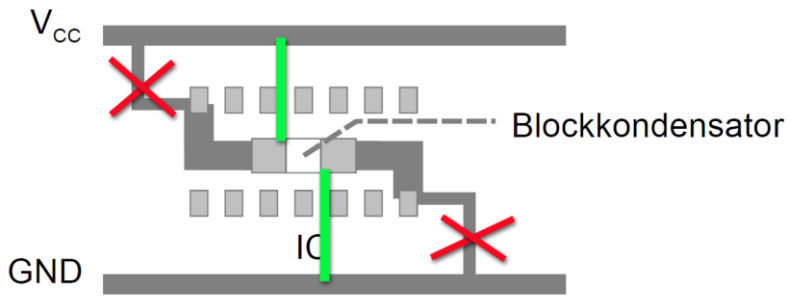


Figure 31: Improved Layout

12 Summary

The measures and information presented in this paper are only an overview about EMC with lining out the most important information. Nevertheless it will be enough for the first confrontation with EMC issues. It summarizes some basic acknowledge about EMC and basic diagnose approaches.

Understanding EMC will take a long time of working on different kinds of issues and lots of experience.

References

[1] Franz, Joachim; EMV – Störungssicherer Aufbau elektronischer Schaltungen, Springer Vieweg, 5. Auflage, 2013

[2] Schlienz, Ulrich; Schaltnetzteile und ihre Peripherie, Vieweg Praxiswissen, 3. Auflage, 2007

[3] STMicroelectronics; http://www.st.com/web/en/resource/technical/document/application_note/CD00222186.pdf, 12.08.2015

[4] Keller, Günther; Elektromagnetische Verträglichkeit bei Schaltnetzteilen, Workshop 36, EMV Stuttgart, 2015